WHAT IS CLAIMED IS:

1. A method for storing data into memory blocks on a programmable integrated circuit configured to implement a user design and operated according to the user design in a user mode, the method comprising:

transferring a first set of data bits from an input pin to a plurality of shift registers on the programmable integrated circuit;

if an enable signal is in a first state, selecting the first set of data bits using a first multiplexer and preloading the first set of data bits into a memory block prior to the user mode; and

if the enable signal is in a second state, preventing the first set of data bits from being preloaded into the memory block using the first multiplexer prior to the user mode.

2. The method as defined in claim 1 further comprising:

transferring a second set of data bits from the input pin to the shift registers on the programmable integrated circuit;

if a second enable signal is in a first state, selecting the second set of data bits using a second multiplexer and preloading the second set of data bits into a second memory block prior to the user mode; and

if the second enable signal is in a second state, preventing the second set of data bits from being preloaded into the second memory block using the first multiplexer prior to the user mode.

3. The method as defined in claim 1 further comprising:

selecting a second set of data bits using the first multiplexer and storing the second set of data bits in the memory block when the enable signal is in a second state during the user mode.

4. The method as defined in claim 3 further comprising:

selecting a first clock signal using a second multiplexer if the enable signal is in the first state, wherein the first set of data is preloaded into the memory block in response to the first clock signal prior to the user mode; and

selecting a second clock signal using the second multiplexer if the enable signal is in the second state, wherein the second set of data is stored in the memory block in response to the second clock signal during the user mode.

5. The method as defined in claim 1 wherein transferring the first set of data bits to the plurality of shift registers further comprises:

transferring the first set of data as serial data on first signal lines;

shifting the first set of data through the plurality of shift registers in response to a first clock signal; and

outputting the first set of data as parallel data from the plurality of shift registers on second signal lines, the first signal lines being less than the second signal lines.

6. The method as defined in claim 5 further comprising:

storing the parallel data in a plurality of flip-flops that are coupled to a second clock signal,

wherein the first set of data is preloaded into the memory block in response to the second clock signal.

7. The method as defined in claim 1 further comprising:

generating first memory address signals using a counter circuit;

selecting the first memory address signals using a second multiplexer if the enable signal is in the first state; and

decoding the first memory address signals, wherein the first set of data bits are preloaded into the memory block prior to the user mode in memory cells selected by the decoded first memory address signals.

8. The method as defined in claim 7 further comprising:

selecting a second set of data bits using the first multiplexer;

selecting second memory address signals generated by logic elements in the programmable integrated circuit using the second multiplexer when the enable signal is in the second state;

decoding the second memory address signals; and

storing the second set of data bits in the memory block in memory cells selected by the decoded second memory address signals when the enable signal is in the second state during the user mode.

9. The method as defined in claim 7 further comprising:

selecting a power supply voltage using a third multiplexer if the enable signal is in the first state; and

providing the power supply voltage to a read/write input of the memory block.

10. The method as defined in claim 1 wherein transferring the first set of data bits from the input pin to the plurality of shift registers further comprises transferring the first set of data bits to the shift registers using a control block.

11. A programmable integrated circuit configured to implement a user design and operated according to the user design in a user mode, the programmable integrated circuit comprising:

a first memory block;

a control block that provides a first enable signal prior to the user mode;

a first register that stores first data bits prior to the user mode if the first enable signal is in a first state; and

a first multiplexer that couples to an output of the first register to a data input of the first memory block if the first enable signal is in the first state, wherein the first data bits are preloaded into the first memory block prior to the user mode only if the first multiplexer selects the first data bits.

12. The programmable integrated circuit according to claim 11 further comprising:

a second memory block, wherein the control block provides a second enable signal prior to the user mode;

a second register that stores second data bits prior to the user mode if the second enable signal is in a first state; and

a second multiplexer that couples an output of the first register to a data input of the second memory block if the second enable signal is in the first state, and the second data bits are preloaded into the second memory block prior to the user mode only if the second multiplexer selects the second data bits.

13. The programmable integrated circuit according to claim 11 wherein the first multiplexer selects second data bits transmitted from logic elements when the first enable signal is in a second state during the user mode.

14. The programmable integrated circuit according to claim 13 further comprising:

a plurality shift registers that convert the first data bits to parallel data, outputs of the shift registers being coupled to inputs of the first register.

15. The programmable integrated circuit according to claim 14 further comprising:

a second multiplexer coupled to programmably select a first clock signal or a second clock signal in response to the first enable signal to provide a selected clock signal, wherein the selected clock signal controls shifting of the first data bits through the shift registers.

16. The programmable integrated circuit according to claim 14 further comprising:

a second multiplexer coupled to programmably select a first clock signal or a second clock signal in response to the first enable signal to provide a selected clock signal, wherein the selected clock signal controls loading data bits into the first memory block.

17. The programmable integrated circuit according to claim 11 further comprising:

a counter circuit that generates first memory addresses; and

a second multiplexer coupled to the counter circuit and an address input of the first memory block,

wherein the second multiplexer programmably selects the first memory addresses or second memory addresses transmitted from one or more logic elements in response to the first enable signal.

18. The programmable integrated circuit according to claim 17 wherein the counter circuit generates a last frame signal when all of the first data bits have been preloaded into the first memory block, a second enable signal changing state in response to the last frame signal causing second data bits to be preloaded into a second memory block prior to the user mode.

19. The programmable integrated circuit according to claim 13 further comprising:

a second multiplexer coupled to a read/write input of the first memory block that programmably selects a supply voltage or a read/write signal in response to the first enable signal, wherein the second multiplexer selects the supply voltage prior to the user mode when the enable signal is in the first state.